Next-Generation Optically-Interconnected High-Performance Data Centers

Wenjia Zhang, Howard Wang, Student Member, IEEE, and Keren Bergman, Fellow, IEEE

(Invited Paper)

Abstract—The communication requirements imposed by the unabated growth in both the size and computational density of modern data centers will soon outpace the fundamental capabilities of conventional electronic interconnection networks. Optical interconnects represent a potentially disruptive technology that can simultaneously satisfy the throughput, latency, and energy demands of these next-generation systems. In this paper, we propose an end-to-end photonic networking platform for future optically-interconnected data center networks. A reconfigurable hybrid photonic network building block and a protocol-agnostic optical network interface comprise the key elements of our proposed system. A modular optical switch fabric prototyping platform is designed and implemented to support a wide variety of potential photonic technologies. We successfully demonstrate nanosecond-scale optical packet-switching at 1-Tb/s per port (40-Gb/s × 25×3) through our prototype, configured as a 4 × 4 switch, and confirm error-free transmission across all wavelengths. In order to flexibly allocate appropriate bandwidth for heterogeneous applications, we further implement and evaluate a novel wavelength-reconfigurable optical packet- and circuit-switch by utilizing our optical switch platform. Finally, we detail our implementation of an optical network interface card (O-NIC) designed to bridge the gap between the well-established protocol layers utilized in current networks and the physical layer of the proposed photonic networks and demonstrate its functionality by the streaming of high-definition video through the end-to-end optical network.

Index Terms—Datacenter, optical communication, packet switching, photonic switching systems.

I. INTRODUCTION

The increasing popularity of cloud-based services continues to drive the creation of larger and more powerful data centers. As these services scale in both number and size, applications oftentimes extend well beyond the boundaries of a single rack of servers. Moreover, the continued advancements in computational density enabled by increasing parallelism in contemporary microprocessors and chip multiprocessors (CMP) have resulted in substantial off-chip communication requirements. As a result, the performance of modern data centers are becoming increasingly communication-bound, requiring upwards of hundreds of thousands of ports supporting petabits per second of aggregate bandwidth [1].

However, due to the super-linear costs associated with scaling the bandwidth and port density of conventional electronic switches, network oversubscription is common practice [2]. Consequently, data-intensive computations become severely bottlenecked when information exchange between servers residing in separate racks is required. In addition, the very nature of the data center as a pool of centralized computational resources gives rise to significant application heterogeneity. The resultant workload unpredictability produces significant traffic volatility, precluding the efficacy of static capacity engineering in these oversubscribed networks. Energy efficiency has also emerged as a key figure-of-merit in data center design [3]. The power density of current electronic interconnects is already prohibitively high—on the order of hundreds of kilowatts—and continues to grow exponentially. As it stands, the power consumption of a single switch located in the higher network tiers can reach upwards of tens of kilowatts when also considering the dedicated cooling systems required. Moreover, measurements on current data center deployments have recorded average server utilization as low as 30% [4], indicating significant wasted energy due to idling hardware starved for data.

As a result, alleviating inter-rack communication bottlenecks has become a critical target in architecting next-generation data centers. The realization of a full bisection-bandwidth, “all-servers-equidistant” interconnection network will not only accelerate the execution of large-scale distributed applications, but significantly reduce underutilization by providing sufficient network performance to ensure minimal idling of power-hungry compute elements. In addition, the increased connectivity between computing and storage resources located throughout the data center will yield more flexibility in virtualization, leading to further enhancements in energy efficiency.

Despite continued efforts from merchant silicon providers towards the development of application-specific integrated circuits (ASICs) for high-performance switches and routers,
the sheer scale of the data center and the relentless demand from data-intensive applications for increased connectivity and bandwidth continues to necessitate oversubscription in hierarchical purely packet-switched electronic interconnection networks. While there have been significant efforts focused on architectural and algorithmic approaches towards improving the overall performance of data center networks [2], [5], these proposals are ultimately constrained by the fundamental limitations imposed by the underlying electronic technologies.

Optical interconnects—capable of ultra-high capacities, bit-rate transparency, distance immunity, and low power density—represent a potentially disruptive solution for overcoming emerging data center network bottlenecks. Recent research advances in photonic devices and switch architectures have enabled transmission capacities on the scale of terabits per second per link with high-radix switching, offering high-throughput interconnectivity for tens of thousands of nodes [7]–[9]. However, optical technologies are traditionally designed for use in telecom applications and thus require significant optimization and reengineering for deployment within a data center environment. As a result, the range of viable optical functionalities—such as switching speed, switching granularity, and connectivity granularity—represents a compelling design space in the context of inserting photonic technologies into what has been a traditionally electronically packet-switched cost-constrained environment [10].

Recently, there have been a number of efforts exploring the viability of circuit-switched optics as a cost-effective means of providing significant inter-rack bandwidth in production data center environments. Helios [6] and e-Through [11] represent two data center network architectures proposing the use of micro-electro-mechanical system (MEMS)-based optical switches. By augmenting existing oversubscribed hierarchical electronic packet-switched (EPS) networks, each implementation realizes a hybrid electronic/optical architecture that leverages the respective advantages of each technology. These initial proposals have successfully demonstrated the potential for utilizing photonic technologies within the context of data center traffic to provide significantly increased network capacities while achieving reduced complexity, component cost, and power in comparison to conventional electronic network implementations. Another network architecture, called Proteus [12], combines both wavelength-selective switching and space switching to provide further granularity in the capacity of each optical link, varying between a few gigabits per second to a hundreds of gigabits per second on-demand.

While network traffic is characteristically unpredictable due to application heterogeneity, communication patterns where only a few top-of-the-rack (ToR) switches are tightly coupled with long, extended data flows have been observed in production data centers [13]. Therefore, the utility of the aforementioned architectures are reliant on the inherent stability of traffic patterns within such systems. Nevertheless, further bandwidth flexibility remains a key target for future data center networks as applications require even higher capacities with increased interconnectivity demands. When studied under the communication patterns imposed by a richer, more representative set of realistic applications, the efficacy of architectures utilizing purely commercial MEMS-based switches, which are limited to switching times on the order of milliseconds, becomes ambiguous [14].

In this paper, we propose a unique end-to-end networking platform for evaluating and implementing next-generation optically-interconnected data center networks. The envisioned photonic platform (Fig. 1) will consist of two enabling subsystems: a reconfigurable network building block supporting a variety of switching functionalities and an optical network interface that will serve to bridge the unique constraints imposed by novel photonic networks with the existing network protocol stack. Through its reprogrammability and functional flexibility, the proposed system represents a ubiquitous platform that will enable the insertion and evaluation of advanced photonic functionalities into existing well-established data center network environments.

In order to empirically assess and validate prospective optical network architectures in an efficient manner, we design and construct a modular optical switch fabric prototyping platform supporting a wide range of photonic technologies, enabling diverse switching speeds (from nanosecond to second scales) and granularities (packet- and circuit-switching). First, we configure the platform as a $4 \times 4$ photonic switch and successfully demonstrate error-free optical packet transmission at 1-Tb/s per port. We then implement and evaluate additional a wavelength-reconfigurable optical packet and circuit-switching testbed. Finally, an optical network interface card (O-NIC) capable of bridging the protocol gap between current computing systems and future
optical networks is developed. We demonstrate its functionality through the streaming of high-definition video, establishing an end-to-end optical system.

II. EXPERIMENTAL NETWORK TESTBED

A. Modular Optical Switch Fabric Prototyping Platform

In order to facilitate increased functionality and to provide straightforward support for future switching technologies, we design and develop a modular optical switch fabric prototyping platform (Fig. 2). This platform consists of a 12 × 12 mainboard (Fig. 2(c)) featuring a field-programmable gate array (FPGA); eight SOA-driver daughterboards (Fig. 2(d)), each containing driver circuitry accommodating two SOAs; eight optical receiver daughterboards (Fig. 2(e)), each supporting two optical receivers; and one peripheral Ethernet interface.

All the receivers and switches on daughterboards are independently connected to the FPGA (Xilinx Virtex 5)—which serves as a central controller providing the desired switching functionality—through sockets on the mainboard. This platform is open to be configured into different types of topology. It also integrates the design of the hybrid packet and circuit-switched photonic router [15] to create a versatile testbed supporting a multitude of functionalities. Moreover, the modular design enables easy adaptability to more advanced switching devices (e.g., PLZT, etc.).

B. 4 × 4 Photonic Switching Node Implemented on a Modular Optical Switch Prototyping Platform

1) Design & Architecture: We configure the modular switch platform into a 4 × 4 SOA-based broadcast-and-select optical space switch (Fig. 3(b)) supporting wavelength-striped optical packets with dedicated frame and header wavelengths (one bit per wavelength) (Fig. 3(a)) [15], [16]. This message format enables extreme simplicity in header detection and routing, achieving minimal latency, decision circuitry complexity, and power consumption [16].

To correctly route optical packets at the scale of nanoseconds, precise engineering of the path length and effective delay of both the electronic and optical paths is of critical importance. In this particular implementation, the latency of the switching node is determined by the sum of the total pigtail fiber delay (e.g., through filters, splitters, combiners, and SOAs) and the electronic delay incurred from signal propagation and processing in the FPGA. In the control path, the optical header propagation latency from input of the switch to the header receiver (Fig. 3(b)) is measured to be 22.5-ns. The delay of the electronics in the control path, as measured from the receiver daughterboard to the SOA daughterboard, is determined to be 16-ns in total. A detailed latency distribution of the electronic path is depicted in Fig. 4. Note that packets will be dropped directly when contention occurs and the latency from contention resolution is not taken into account. Lastly, there is a final 12.2-ns of delay attributed to the fiber lengths of the SOA and passive combiner. A customized filter, splitter, and delay module is used in the data path to precisely match the latency incurred through the control path, ensuring the simultaneous arrival of the electronic gating signal and the optical packet at the SOA.

Power consumption for this switch prototyping platform is also experimentally measured. All the mainboard, SOA-based switch and optical receiver daughterboards operate at 5 V. While the current of the motherboard is about 0.35 A, the receiver daughterboard is also about 0.35 A and the switch daughterboard is about 0.6 A. Therefore, the total power consumption of this switch platform is about 40 W. If each port
operating at 1-Tb/s, the power efficiency of this switch is about 10-pJ/bit.

To demonstrate the correct routing functionality for the 4 × 4 switch, we switch the wavelength striped optical packets to each output of the switch according to the 2-bit address encoded on the header wavelengths. The waveforms in Fig. 5 depict packets correctly propagating from a representative input port to each of the four outputs, confirming routing correctness through the switch.

2) 1-Tb/s/Port (40-Gb/s × 25) Packet Switching: The ever-increasing demand for high-bandwidth communication is driving the need for technologies that can provide substantial increases in link capacity to support the node throughputs of future data center systems. While research in fiber link transmission has achieved significant progress in recent years—multicore fiber transmission operating at over 100-Tb/s was demonstrated in [17]—the throughput attainable by optical switches have not scaled commensurately. Recent work has demonstrated 2.56-Tb/s per port capacities using a dual-polarization DWDMDQPSK (20-Gb/s × 64λ × 2 pol.) format transmitted through a PLZT-based 2 × 2 optical packet switch system [18]. Unfortunately, as a result of the complicated modulation and demodulation schemes, the limited durability of the required devices precludes the use of such a system in large-scale computing environments. The authors of [19] have experimentally demonstrated packet switching using both 8 × 40-Gb/s on-off keying (OOK) and differential-phase-shift-keying (DPSK) through an optical network testbed. However, the 4 × 4 switch architecture used suffers from internal blocking, limiting its effective switching capacity.

In order to verify the capability of the proposed architecture as a high-speed-throughput switching platform, we demonstrate 1-Tb/s per port (40-Gb/s × 25λs) through this non-blocking 4 × 4 packet switch. Fig. 6 depicts the experimental setup for our 4 × 4 optical packet switching system. Twenty-five C-band continuous-wave (CW) DFB lasers—ranging from 1535.82 nm to 1558.17 nm—are multiplexed onto a single fiber and simultaneously modulated by a 40-Gb/s, 2^{15} – 1 pseudorandom bit sequence (PRBS) originating from a pulse pattern generator (PPG). The multiplexed CW light is attenuated prior to the modulator to avoid damage from excessive optical power at its input. The modulated data wavelengths are subsequently decorrelated by 1.5-km of standard single mode fiber (SSMF). Using SOAs driven by an Agilent ParBERT, wavelength-striped packets are generated by independently gating a frame wavelength, two header wavelengths, and the modulated data wavelengths into 90-ns long packets with a 96-ns period. These optical packets are then injected into the 4 × 4 switch and routed based on the address information encoded on the header wavelengths. Each data wavelength is isolated by a tunable filter and amplified by an erbium-doped fiber amplifier (EDFA). In order to limit the effect of the EDFA’s wavelength-dependent gain profile on data verification, a variable optical attenuator (VOA) is placed before the tunable filter to provide a means for power equalization. Another tunable filter is placed downstream from the EDFA for the purpose of reducing amplified spontaneous emission (ASE) noise introduced by the amplifier. The signal passes through a final VOA before being received by a PIN photodiode and transimpedance amplifier (TIA) assembly. The recovered 40-Gb/s data segments are electronically demultiplexed down to 10-Gb/s to be examined by a 12.5-Gb/s bit-error rate tester (BERT). A data communication analyzer (DCA) is used to examine the temporal performance of the link while two optical spectrum analyzers (OSAs) monitor the output of the initial tunable filter and of the switch. A common 10-GHz clock source synchronizes the ParBERT, PPG, BERT, and DCA.

To optimize switching performance and minimize inter-channel crosstalk, we first determine the dynamic range of the input power per channel (P_{ch}) for the channels corresponding to 1535.82 nm, 1545.32 nm, and 1558.17 nm. A second-degree polynomial trend line is fitted onto the measured power penalty data, determined at a BER of 1 × 10^{-9}. Examination of the results shown in Fig. 7 indicate that the range of P_{ch} corresponding to a relative power penalty of less than 1-dB for these three wavelengths is wider than 4-dB, establishing an optimized P_{ch} range for our twenty-five-wavelength implementation, and verifying the viability of ultra-bandwidth switching across an SOA-based switch fabric.

We further validate the performance of our switch by measuring and recording the BER of four representative wavelengths evenly spaced across the spectrum of the twenty-five payload channels, each at 40-Gb/s. Eye diagrams for these four wavelengths are shown in Fig. 8(b). The spectrum of the
wavelength-striped data, frame, and header channels are depicted in Fig. 8(a). Fig. 9 plots the recorded BER curves taken on the packetized data. We observe error-free operation for each wavelength and measure power penalties approximately ranging between 0.7-dB to 1.5-dB.

Due to carrier density variations, saturation effects, and inter-channel nonlinear effects in the SOA, the multi-wavelength packets suffer from significant waveform distortion under switching. As a result, the power penalties measured in this experiment are higher than those observed in [19]. The observed power penalty (BER at $10^{-9}$) for twenty-five wavelengths is also recorded in Fig. 10, indicating that power penalties for the majority of the wavelengths are less than 1-dB. The high power penalties at 1530 nm and 1550 nm can be attributed to the high noise figure of the SOA and EDFA under switching and amplification, respectively.

C. Wavelength-Reconfigurable Optical Packet and Circuit-Switched Platform for Data Center Networks [20]

Bandwidth flexibility and availability are key challenges for photonic interconnects in data center networks. In order to flexibly allocate appropriate bandwidth for heterogeneous applications, we propose a wavelength-reconfigurable optical packet and circuit-switched network architecture enabling multi-granular interconnectivity at nanosecond-scale switching speeds. Previous work presented in [15] experimentally demonstrates a photonic switch supporting both packet and circuit switching at the granularity of each port. In this work, we integrate a wavelength selective switch (WSS) into the design of [15], illustrating the potential for supporting hybrid switching functionality at sub-wavelength granularities through dynamic wavelength provisioning.

The design for a $2 \times 2$ wavelength-reconfigurable switching module is illustrated in Fig. 11 and consists of two WSSs along with the aforementioned packet and circuit-switching optical switch platform. In this design, wavelength-striped packets are
individually routed based on the address encoded on the bit-parallel headers. However, when a long-lived and high-QoS application requires use of the network a pre-selected combination of wavelengths, previously assigned to carrying packet payloads, are re-allocated for use as circuit paths. This is accomplished by routing these wavelengths to the circuit switching subsystems via an appropriate configuration of the WSS. The centralized FPGA controller is used to manage output contentions and delivers the appropriate routing information to each switch and is also able to accept incoming configuration information, which indicates the wavelengths to be used for circuits or packets, from the ports on the motherboard in a manner similar to that in [15]. As a result, this architecture simultaneously supports both optical packet and circuit traffic at the granularity of individual wavelengths as enabled by WSS.

In order to validate the feasibility of our proposed design, we construct a testbed comprised of our modular switch platform and an Optoplex 3-port tunable optical add/drop multiplexer (TOADM) as a WSS. As shown in Fig. 11, the modular switch platform is configured as a $4 \times 4$ SOA-based broadcast-and-select optical space switch, wherein the top two input ports carry optically-addressed packets while the remaining two input ports carry circuit-switched traffic. Eight C-band 100 GHz-spaced CW lasers, with wavelengths ranging from 1542.94 nm to 1548.51 nm, are combined using a coupler and simultaneously modulated with 10-Gb/s $2^{11} - 1$ PRBS pattern, which is subsequently decorrelated by 10-km of SMF. The control wavelengths—including one frame and two headers—are gated independently using SOAs driven by an Agilent ParBERT and combined with the data channels to form 89.6-ns-long wavelength-striped optical packets with a period of 102.4 ns. The resulting packets are injected into the TOADM and then switched through the SOA-based switching fabric. Optical circuits are generated on the same wavelengths and transmitted in a similar fashion. At the output of the network, we extract each 10-Gb/s channel using a tunable filter followed by an EDFA, after which another tunable filter is used to limit ASE noise. The extracted signal passes through a VOA and is received by a PIN-TIA with an integrated limiting amplifier (LA) to be examined on a BERT.

First, we confirm that the $8 \times 10$-Gb/s optical payloads are correctly routed through the switch fabric. We then experimentally confirm that all the egressing optical packets and circuits achieve error-free transmission (defined as a BER less than $10^{-12}$). Eye diagrams of a representative channel (C42, $\lambda = 1543.73$ nm) under packet switching from both the input and output of the switch are recorded in Fig. 12(a)–(b). The BER curves in Fig. 13(a) show an approximately 0.8-dB power penalty for packets routed through the switch fabric. Next, 10-Gb/s input and output eye diagrams corresponding to the
Fig. 16. Optical Network Interface Card Architecture.

III. NETWORK INTERFACE FOR MULTI-WAVELENGTH OPTICAL INTERCONNECTION NETWORKS

Standardized electronic communications protocols—such as PCI Express, InfiniBand, and Ethernet—have been pivotal in enabling interoperable connectivity between compute nodes at considerable scales. While significant strides in photonic network architectures have been made, switching at the granularity of messages in the optical domain represents a fundamentally unique physical layer operation that violates the conventional view of layer one as a static link. This incompatibility with existing communication infrastructures is a critical hurdle for optically-switched networks that must be overcome to enable their adoption within practical, real-world computing systems. Therefore, there is a critical need for the creation of a network interface that can seamlessly bridge the protocol divide between the electronic end nodes and the optical network.

To this end, we propose the design of an optical network interface card (O-NIC) capable of delivering a transparent view of the underlying interconnect to the end node [21]. Our envisioned platform will achieve this transparency through the abstraction of the optical network as a virtual switch (Fig. 15). As a result, the end node will recognize and communicate with the optical network as if it were a high-radix switch compliant with the local node’s communication protocol of choice. Each O-NIC serves to transparently translate addressing, flow control, and management information, while also providing the necessary burst-mode WDM physical layer interface to the optics.

A. 10-GE Based Optical Network Interface Card

We implement our 10-Gigabit Ethernet (10GE) O-NIC prototype on a development board featuring a high-speed field-programmable gate array (FPGA). Via its 10-Gigabit Attachment Unit Interface (XAUI), the development board connects to a commercial 10GE NIC residing on a host computer. The XAUI supports four lanes of 8 b/10 b encoded 3.125-GBaud signals capable of an aggregate rate of 10 Gb/s.

Fig. 16 illustrates the logic design of the O-NIC as implemented in the FPGA. At the host, the PC generates an Ethernet packet stream, which is transmitted through the XAUI to the O-NIC where it is deserialized, aligned, and 8b/10b decoded in the 10GE link layer transceiver. The data is then passed to self-defined modules that are responsible for parsing the Ethernet header, transferring the data between clock domains, and buffering data packets. The data is then encoded in our wavelength-striped packet format. A virtual network function module transparently translates the extracted Ethernet addresses into optical routing information, which is subsequently mapped onto dedicated optical header wavelengths. At the same time, network statistics are submitted to a management server through a network measurement interface. Simultaneously, each lane of the XAUI-based Ethernet payload is modulated onto optical data channels (in this implementation, channels C36 through C39 of the ITU grid). The 4 x 3.125-Gb/s optical data are transmitted over optics, with link training via Align/Sync/Idle sequences (K28.0, K28.3, and K28.5) transmitted during channel idle times.

B. Experimental Demonstration

The experimental setup (Fig. 17(a)) consists of two 10-Gb/s Myri-NIC equipped 64-bit PCs connected via two O-NICs through an optical link. The Ethernet packet stream generated from the host computer is connected to an Altera Stratix II GX-based FPGA development board through transceivers configured for the XAUI protocol. The transceivers drive four LiNbO₃ modulators, mapping the data onto four optical channels, namely 1548.51 nm (C36), 1547.72 nm (C37), 1546.92 nm (C38), and 1546.12 nm (C39). At the receiver, the data is recovered at the transceivers of the second FPGA through PIN photodetectors followed by transimpedance and
limiting amplifiers. A DC block is inserted inline to achieve the AC coupling required by the development board. A standard 156.25 MHz reference clock, used by the FPGAs, is provided by a signal generator and RF splitter. The upstream traffic is looped back using electronic links.

In order to verify signal integrity, eye diagrams of the payload channels are recorded at the electronic transmitters, optical transmitters, and electronic receivers. The open eye diagram of one representative channel is shown in Fig. 17(b), confirming signal quality through the interface and optical link.

Next, end-to-end functionality is demonstrated by streaming HD video between a VLC server and client across the O-NICs and optics. Fig. 18 depicts screen shots captured at each host. The video stream is transmitted without distortion or frame loss, verifying that the interface is performing as designed. We also disconnect the optical link manually and then reconnect after several seconds, resulting stoppage of the video and subsequent resumption as soon as the link is restored, demonstrating the robustness of this O-NIC design in dealing with the presence of link failures.

IV. CONCLUSION

We propose an end-to-end photonic networking platform for future optically-interconnected data center networks, featuring with a reconfigurable hybrid photonic network building block and a protocol-agnostic optical network interface. A 4 × 4 photonic switch is designed and constructed by configuring a modular optical switch fabric prototyping platform and error-free optical packet transmission at 1-Tb/s per port is successfully demonstrated. Then, we implement and evaluate a wavelength-reconfigurable optical packet- and circuit-switching testbed. Furthermore, we successfully demonstrate the setup of an end-to-end link and HD video transmission via the proposed 10GE O-NIC assisted optical testbed.

Optical interconnects is a disruptive solution for the data center networks offering ultra-high bandwidth, low latency and reduced power consumption. And there’s a range of viable optical functionalities representing a compelling design space in the context of inserting photonic technologies into electronically interconnected networks. This proposed end-to-end system provides a programmable platform for empirically assessing and validating prospective optical network architectures for next generation data center system.

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REFERENCES


Wenjia Zhang (S’09) received the B.S.E. degree in communication engineering from Beijing University of Posts and Telecommunications (BUPT), Beijing, in 2007. He visited the Lightwave Research Laboratory at Columbia University from September 2010 to March, 2012 and is currently pursuing the Ph.D. degree in communication and information system at BUPT.

His research interests include optical burst switching networks, cross-layer optimization in optical networking and optically interconnected data centers.

Howard Wang (S’05) received the B.S. and M.S. degrees in electrical engineering from Columbia University, New York, NY, in 2006 and 2008, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include the design of photonic interconnection network architectures for advanced computing systems and optically interconnected data centers.

Keren Bergman (S’87–M’93–SM’07–F’09) received the B.S. degree from Bucknell University, Lewisburg, PA, in 1988, and the M.S. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, in 1991 and 1994, respectively, all in electrical engineering.

She is currently the Charles Batchelor Professor and Chair of Electrical Engineering at Columbia University where she also directs the Lightwave Research Laboratory She leads multiple research programs on optical interconnection networks for advanced computing systems, data centers, optically interconnected memory, and chip multiprocessor nanophotonic networks-on-chip.

Dr. Bergman currently serves as the co-Editor-in-Chief of the IEEE/OSA JOURNAL OF OPTICAL COMMUNICATIONS AND NETWORKING and is a Fellow of the OSA.